

Amendments to the Specification

Please **replace** the paragraph beginning at **page 3, line 30**, with the following **amended** paragraph:

Referring to FIG. 1, a block diagram of an exemplary embodiment of television signal processing apparatus 100 is shown. In FIG. 1, television signal processing apparatus 100 comprises signal receiving means such as signal receiving element 110, tuning means such as tuner 130, demodulation means such as demodulator 140, decoding means such as decoder 170, processing means and memory means such as processor and memory 180, audio amplification means such as audio amplifier 190, audio output means such as speaker 135, video processing means such as video processor 145, and visual output means such as display 155, ~~a power supply 125 and a switch 115 responsive to said processor and memory 180.~~ Some of the foregoing elements may for example be embodied using integrated circuits (ICs). For clarity of description, certain conventional elements of television signal processing apparatus 100 including control signals may not be shown in FIG. 1. According to an exemplary embodiment, television signal processing apparatus 100 may receive and process signals in analog and/or digital formats.

Please **replace** the paragraph beginning at **page 7, line 7**, with the following **amended** paragraph:

Referring to FIG. 4, a diagram of a clock divider circuitry 400 of a clock generator according to an exemplary embodiment of the present invention is shown. In FIG. 4, the clock divider circuitry 400 comprises a plurality of D flip-flops 405, 410, 415, 420, 425, 460, 465, 470, a plurality of AND gates 430, 435, 440, 445, a plurality of OR gates 450, 455 fates 250, 255. In the exemplary embodiment of the present invention shown in Fig. 4, five D flip-flops 405, 410, 415, 420, and 425 are used to create a delay line for the reference clock. The PLL clock is used to advance the state of the delay line. The group of logic elements comprising the AND gates 430, 435, 440, 445 and the OR gates 450, 455 are used as a means for comparing the various output stages of the delay line 405, 410, 415, 420, 425. For example, to generate the 1X clock, the state of the outputs of the first D flip-flop 405, the second D flip-flop 410, the fourth D filp-flop 420, and the fifth D flip-flop are compared using the group of logic elements 430, 435, 440, 445, 450, 455. The 1X clock is

then passed through a final D flip-flop 460 to complete the synchronization of the reference clock with the PLL clock.